THAT WHICH IS CLAIMED IS:

1. A sensing circuit for a memory cell inserted between a first and a second voltage reference and connected, in correspondence with a first inner circuit node, to said memory cell of the type comprising:

- a first bias current generator inserted between said first voltage reference and said first inner circuit node;

- a comparator having a first input terminal connected to a comparison circuit node, connected in turn to said first voltage reference by means of at least a second reference current generator, as well as a second input terminal connected to a circuit node connected in turn to said first inner circuit node, an output terminal of said comparator corresponding to an output terminal of said sensing circuit;

characterised in that it comprises also:

- a cascode-configured bias circuit inserted between said inner circuit node and said matching circuit node and connected to a third voltage reference; and

- a current/voltage conversion stage connected to said matching circuit node and to said comparison circuit node, as well as to said second voltage reference.

2. A sensing circuit according to claim 1, characterised in that said cascode-configured bias circuit comprises a transistor inserted between said inner circuit node and said matching circuit node as

well as an operational amplifier having a first input terminal connected to said third voltage reference and a second input terminal feedback-connected to an output terminal, connected in turn to a control terminal of said transistor.

3. A sensing circuit according to claim 2, characterised in that said transistor is of the P-channel MOS type.

4. A sensing circuit according to claim 1, characterised in that said current/voltage conversion stage comprises a first transistor, diode-configured and inserted between said matching circuit node and said second voltage reference, as well as a second transistor, inserted between said comparison circuit node and said second voltage reference and having a control terminal connected to a control terminal of said first transistor.

5. A sensing circuit according to claim 4, characterised in that said first transistor and said second transistor are of the N-channel MOS type.

6. A sensing circuit according to claim 1, characterised in that it comprises a plurality of branches comprising a plurality of reference current generators connected to a plurality of inputs of said comparator having a plurality of output terminals.